We claim:

1. A cache memory, comprising:

addresses split into a tag part, an index part and an offset part; and

means for performing a transformation between the tag part of an address and a coded tag address being unambiguous in both directions.

2. The cache memory according to claim 1, wherein said means performs a transformation between the index part of the address and a coded index address that is unambiguous in both directions.

3. A method for addressing a cache memory, which comprises the step of:

performing a transformation between a tag part of a cache address and a coded tag address being unambiguous in both directions.

4. The method according to claim 3, which further comprises performing a transformation between an index part of the cache address and a coded index address being unambiguous in both directions.

5. A cache memory, comprising:

addresses split into a tag part, an index part and an offset part; and

a transformation device performing a transformation between the tag part of an address and a coded tag address being unambiguous in both directions.

6. The cache memory according to claim 5, wherein said transformation device performs a transformation between the index part of the address and a coded index address that is unambiguous in both directions.